Portfolio
Toronto, Canada

Jimmy Velasco

jimmy.velascogranda@mail.utoronto.ca

LinkedIn
(437) 229-8576

Education

University of Toronto
BASc. Electrical & Computer Engineering

Minors
AI & ML
Robotics and Mechatronics

Certificate
Entrepreneurship and Innovation

Skills

Python
C/C++
MATLAB
Altium
Verilog/SV
PyTorch
SciKit
Vivado

Courses

Hardware Design
DSA
Deep Learning
Signals & Systems

Experience

Digital Designer - Software Developer — **Tesla Inc** — Sept 2024 - Jan 2025, Palo Alto, CA

- Migrated SoC component codebase to **SystemVerilog**, introducing a modular distributed structure and intuitive interfaces; reduced code size by 45%, boosted scalability by 30%, and improved feature development productivity by 17%.
- Developed a **custom NoC communication simulator** in Python with a modular, well-documented codebase; enabled early-stage algorithm validation in software prior to hardware implementation. Deployed as an internal tool on the company network.
- Conducted **performance modeling** for custom NoC communication algorithms using the internal simulator; identified bottlenecks and approximated hardware characterization to guide architectural improvements and boost efficiency.
- Co-developed a custom **DFT** solution in SystemVerilog, integrating multiple Tessent **MBIST** controllers to support complex memory configurations; conducted behavioural pre-validation in **cocotb** to ensure robust verification coverage.

Digital Design Verification - Software Developer — **AMD Inc** — May 2023 - Aug 2024, Toronto - Canada

- Developed repeaters contract script for identifying interfaces with clock gating, format conversion and control signals sanity checks.
- Maintained sanity, IP and power analysis regressions as well as DC Elab and Lint checks for different VCN versions and variants.
- Automated VCN system blocks regression runs for regular running and reporting and IP release flow for SoC enablement.
- Contributed graphics encoder design verification by setting up a **UVM** test bench utilizing SystemVerilog and **Verdi**.
- Automated report generation of power analysis fsdb files using **Python** and verified their correctness through **Verdi**.

Projects

Software Developer — **PLLpy Simulator** — 2025

- Developed a high-level **PLL simulator** in Python for rapid system characterization, achieving up to **8X faster simulation** performance compared to equivalent Matlab implementations.
- Implemented key features including waveform visualization, parameter sweeping, configuration parsing, and **modular vectorized components** to enhance usability and flexibility.
- Designed the simulator to support multiple loop filters (R, RC, RCC) and integrated SerDesPy for CDR analysis.
- Published the tool as an open-source package on **PyPI** with comprehensive documentation and tutorials; structured for easy extension with new modules, filters and components.

Machine Learning Researcher — **TasteBud** — 2023
Recipe Generator

- Teamed up with a group of four to develop an AI model that generates food recipes based on a list of ingredients.
- Developed and implemented the datasets' processing logic to ensure compatibility between recipes, ingredient lists and cuisine types using **Python** (**Pandas**, **Numpy**).
- Created an ingredient compatibility adjacency matrix and for analyzing 2.23 million recipes.
- Constructed and analyzed the performance of a **PyTorch**-based **RNN** (GRU) and a **GAN** architecture for generation.

Embedded Systems Designer — **Handy** — 2023
Hand-Controlled Canvas

- Designed a wireless hand-motion-based controller, using 2 SMT32 **MCUs** to interconnect an **IMU** with multiple sensors and intercommunicate them through **I2C**, **SPI**, **UART**, and IEEE 802.15 protocols.
- Devised and implemented a **C** algorithm to control variable-size digital pointer through a 6-DoF IMU, and a flex sensor
- Enabled wireless remote control capabilities by interconnecting HC-05 Bluetooth to the main SMT32 MCU.
- Developed and deployed a **Python**-based drawing canvas to showcase the hand-control capabilities of the device.
- Optimized the frame generation algorithm through the built-in STM32 **DMA** and improved frame reconstruction by implementing data truncation and Run-Length Encoding (RLE), reaching 64 FPS average in B/W.

Digital Designer — **ARM Cortex A9 Processor** — 2022

- Developed and synthesized an 11-instructions processor compliant with **ARM Cortex-A9** architecture using **Verilog**.
- Enhanced the processor to support DE1 **FPGA** interfaces for LED decoding, switch control, and 7-segment display.
- Showcased capabilities through an assembly memory game controlled by DE1-SoC switches, LEDs and display.

Design Teams

Robotics Designer — **RSX UofT** — 2023
Space Rover

- Devised motor controller after identifying the optimal motor, encoder, and gearbox combination for URC missions.
- Developed custom schematics and a 3-layer PCB for the gripper's brushed DC motor driver using H-bridge architecture (IFX007T) and **SMT32** "blue pill" using **KiCad** and **Altium**.
- Developed and implemented a **PID** controller in **C** for **CAN** communication system.
- Engineered supports for integrating the PCB controller within the rover's framework, leveraging **Fusion 360**.

Aero/Electrical Team — **Blue Sky UofT** — 2021 - Present
Solar Racing Car

- Revamped steering wheel schematics and **PCB** layout for Gen12 using **Altium**. The redesign focused on compatibility with the new centralized BFM and streamlining the driver's interaction by reducing inputs, adding button types and adding an LCD screen.
- Debugged and validated the custom **STM32** PCB, which controls extended features at the steering wheel, employing **C** in **CubeIDE** and **Keil**.
- Overhauled, diagnosed and repaired the side panel PCB with auxiliary functionalities using power supplies, wave generator, **oscilloscopes**, multimeter, and **soldering** station.
- Generated canopy meshes for aerodynamic simulation utilizing **Pointwise** and small part design in **CATIA**.